



Tiempo ACC (Asynchronous Circuit Compiler) is the first synthesis tool which automatically generates asynchronous and delay-insensitive circuits from a model written in a standard hardware description language.

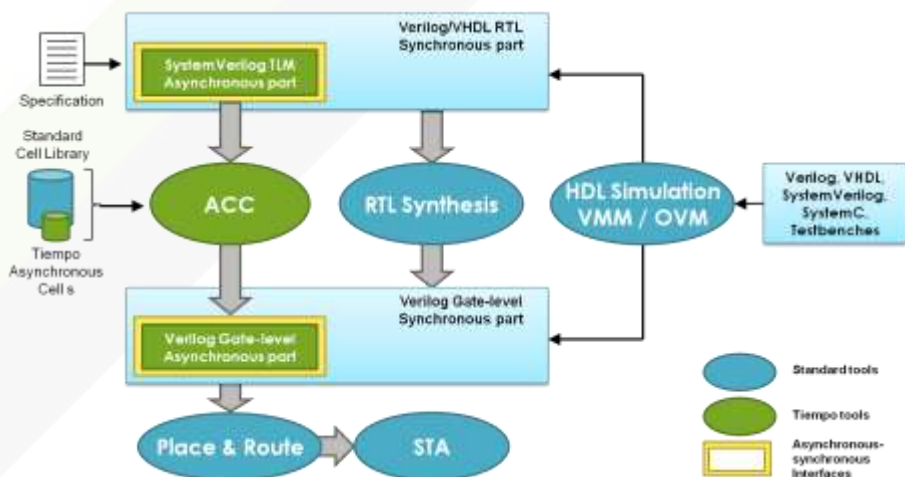
### Overview

ACC takes as input a description written in SystemVerilog TLM, which is perfectly suited for high-level modeling of clockless circuits, and generates as output a gate-level netlist in standard Verilog format. ACC can be inserted in any standard design flow, allowing designer to verify asynchronous and mixed asynchronous/synchronous circuits using any industry-standard simulation tool. The generated Verilog netlist can then be placed-and-routed using any standard back-end tool and verified with any electrical simulation tool.

ACC is available as an optional license attached to any Tiempo core IP license, allowing customers to independently modify the purchased IPs as well as to synthesize their specific asynchronous blocks complementing these IPs.

Targeted applications are chips for smart cards (with or without contact), RFID tags, sensor networks, systems embedding NFC technology and other secured applications.

### ACC in standard design flow



## Key features

- Fully automated synthesis tool
- Standard hardware description languages
  - Input: SystemVerilog TLM-like model
  - Output: Verilog gate-level netlist
- Fully integrated in standard EDA flows
- Tool license attached to IP license (option)

## Key benefits

- ACC\_Check tool allows checking that the SystemVerilog description is compatible with ACC coding style
- ACC timing engine allows delivering standard SDC files to comply with back-end STA checks
- Multiple optimization options to deliver a netlist with minimal power and/or maximum performance
- Automatic generation of synchronous/asynchronous interfaces
- Fully compatible with standard simulation tools

